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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/992,222	12/17/97	HOBBS W	INPA:056

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LM12/0517

EXAMINER

DAVIS, T

ART UNIT	PAPER NUMBER
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2781

DATE MAILED: 05/17/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.
08/992,222

Applicant(s)
Hobbs et al.

Examiner
Theresa L. Davis

Group Art Unit
2781



☒ Responsive to communication(s) filed on Apr 1, 1999

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire three(3) month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-28 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-28 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

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DETAILED ACTION

1. Claims 1-28 are presented for examination.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

4. Claim rejected under 35 U.S.C. 102(b) as being anticipated by Pawlowski, Patent No. 5,696,910.
5. As per claim 1, Pawlowski teaches the invention as claimed including at least one instruction memory storing a predefined bus stimuli instruction (col. 3, lines 1-5); and at least one phase generator coupled between the bus and the instruction memory for providing signals to the bus in response to the instruction (col. 1, lines 57-65).

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6. As per claim 2, Pawlowski teaches the invention as claimed including the instruction memory storing a plurality of predefined bus stimuli instructions (col. 1, lines 59-61).
7. As per claim 4, Pawlowski teaches the invention as claimed including the phase generator is responsive to signals received from the bus (col. 3, lines 53-58).
8. As per claim 5, Pawlowski teaches the invention as claimed including a response memory coupled to the phase generator storing predefined responses to signals received from the bus (col. 6, lines 31-36).
9. As per claim 6, one digital logic device responsive to the instructions and at least one phase engine for controlling timing of the bus stimuli (col. 7, lines 33-41).
10. As per claims 7 and 8, "Official Notice" is taken that both the concept and the advantage of having field programmable gate arrays and application specific integrated circuits are common and well known in the art.
11. As per claim 12, Pawlowski teaches the invention as claimed including a system phase engine, an arbitration phase engine, a request phase engine, a snoop/error phase engine, and a data phase engine (col. 5, lines 11-25).
12. As per claims 16-20, see above rejected claims 1-6. The same rationale is use here.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. Claims 3, 9, 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pawlowski, Patent No. 5,696,910 and further in view of Cloutier, Patent No. 5,892,962.

15. As per claim 3, Pawlowski does not specifically teach of the instruction comprises an instruction word having a predefined length. However, Cloutier teaches of the instruction comprises an instruction word having a predefined length (col. 5, lines 53-60).

16. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the teachings of the Cloutier system withing the Pawlowski system to improve the accuracy and flexibility of the storage involved. Furthermore, both references deal with the same art in the field of computers. Therefore, it would have been obvious to one of ordinary skill in the art to modify the Pawlowski teachings to obtain the claimed invention.

17. As per claims 9, 13, and 14, Pawlowski does not specifically teach of the digital logic device which includes a control portion for providing bus control signals and a data portion for sending data to the bus; a data memory coupled to the data portion; a data portion which receives data from the bus However, Cloutier teaches of a digital logic device which includes a control portion for providing bus control signals and a data portion for sending data to the bus (col. 3, lines 64-col. 4, line 6); a data memory coupled to the data portion (col. 5, lines 53-54); a data

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portion which receives data from the bus (col. 5, lines 53-54). The same rationale for combination of references applies here as to above claim 3.

18. As per claim 10, Cloutier further teaches the control portion includes a flow logic device, a request logic device, and a data logic device (col. 3, lines 50-63). The same rationale for combination of references applies here as to above claims 3, 9, 13, and 14.

19. As per claim 11, Cloutier further teaches at least one logic level translation device (col. 8, lines 63-67). The obviousness to combine these references can be seen in the above claims 3, 9, 10, 13 and 14. The same rationale applies here.

20. As per claim 15, Pawlowski teaches an instruction memory storing digital data representing predefined bus stimuli (col. 3, lines 1-5); a system protocol generator coupled to the bus and the flow logic device (col. 7, lines 42-46); an arbitration protocol generator coupled to the flow logic device and the bus (col. 5, lines 37-43); a request protocol generator coupled to the flow logic device, the request logic device and the bus (col. 5, lines 44-48); a snoop/error protocol generator coupled to the request logic device and the bus (col. 5, line 54-col. 6, line 30); a data protocol engine coupled to the data logic device (col. 5, lines 25-33); a transaction response memory coupled to the flow device and the request logic device storing digital data representing predefined responses to signals received from the bus (col. 6, lines 30-67). Cloutier teaches a flow logic device responsive to the instruction memory (col. 3, lines 33-63); a request logic device responsive to the instruction memory (col. 3, lines 38-40); a data logic device responsive to the instruction memory (col. 3, lines 40-45); a data memory coupled to the data

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logic device storing data to be exchanged with agents on the bus (col. 3, line 41). The obviousness to combines these references can be seen in the above claims 3, 9-11, 13 and 14.

The same rationale applies here.

21. Method claims 21-28 are rejected as referenced and applied to apparatus claims 1, 15, and 16 above.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wiseman et al., Patent No. 5,802,317; Trimberger, Patent No. 5,752,035, Hotchkin, Patent No. 5,727,218, Gulick et al. Patent No. 5,748,983, Blamer et al. 5,659,722.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa L. Davis whose telephone number is (703) 305-0624. The examiner can normally be reached on Monday-Thursday from 7:30 to 5:00. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh, can be reached on (703)305-9648. The fax phone number for the organization where this application or proceeding is assigned is (703)308-3718.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Theresa L. Davis

5/7/99


AYAZ R. SHEIKH
SUPERVISORY PATENT EXAMINER
GROUP 2700